



Application No.: 09/835,643
Amendment dated May 22, 2003
Reply to Office Action of March 19, 2003

Docket No.: M4065.0383/P383

REMARKS IN RESPONSE TO THE OFFICE ACTION

Claims 1-44 and 110 are now pending in this application. Claims 1, 2, 4, 6, 9, 13-18, 20, 28, 33 and 41 have been amended. Claim 110 has been added. No new matter has been added. Applicants reserve the right to pursue the original claims and other claims in this application and in other applications.

Applicants acknowledge with appreciation the allowance of claims 19-44. Applicants also note with appreciation the allowance of claims 4-9 and 12-18, if rewritten in independent form. Accordingly, claims 4, 6, 9 and 14-18 have been rewritten in independent form to include all limitations of the base claim and any intervening claims. Rewritten independent claim 4 is now the base claim of claims 5, 7, 8, 12, and 13.

Claims 13, 28, and 41 have been similarly amended to broaden the scope of the claims. These amendments are supported by paragraph 31 of the specification, which states in part that the “substrate 12 may be exposed to a dilute silane at a temperature of about 300 °C to form a thin surface silicide layer 24 (Figure 7) on each of the exposed sidewalls of the conductive material.”

Claim 110 has been added and includes all limitations of amended independent claim 1.

Claims 1-3 stand rejected under 35 U.S.C. §102(b) as being anticipated by Lu et al. (U.S. Patent No. 5,429,978) (“Lu”). This rejection is respectfully traversed.

The claimed invention relates to a method of forming a low-loss coplanar waveguide. As such, amended independent claim 1 recites a method of forming “a coplanar waveguide” by *inter alia* “forming a signal conductor line over a substrate” and “forming two longitudinal ground conductor planes over said substrate and on opposing sides of said signal conductor line.” Amended independent claim 1 further recites

“subsequently forming a trench in said substrate in an area between at least one of said ground conductor planes and said signal conductor line.”

Lu relates to a method for fabricating a high density self-aligned dynamic random access memory (DRAM) cell having a stacked capacitor structure in a trench. (Col. 1, lines 7-12) As such, Lu teaches forming a field effect transistor (FET) and an interconnection spaced apart from one another. (Col 3, line 39, FIG. 1) According to Lu, gate electrodes for the FET and interconnect are formed by forming a gate oxide layer on a substrate and a field oxide region, depositing a polysilicon layer on the gate oxide layer, forming a silicon oxide layer over the polysilicon layer, and patterning the three layers. (Col. 3, lines 35-50). Lu further teaches forming a trench between the FET and interconnection and forming a capacitor in the trench. (Col. 3, lines 57-66).

Lu fails to disclose all limitations of independent claim 1. Specifically, Lu fails to teach or suggest a “method for forming a coplanar waveguide” by “forming two longitudinal ground conductor planes over said substrate and on opposing sides of said signal conductor line,” as recited in amended independent claim 1. Lu teaches only forming a DRAM cell by forming a FET spaced apart from an interconnection. According to Lu the FET and interconnect each include a layer of polysilicon and the layers of polysilicon are spaced apart from each other. Lu, however, is silent about a “method for forming a coplanar waveguide” by *inter alia* “forming two longitudinal ground conductor planes over said substrate and on opposing sides of said signal conductor line,” as recited in amended independent claim 1. Since Lu fails to teach all limitations of amended independent claim 1, withdrawal of this rejection is respectfully requested.

Claims 10 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lu in view of Gardner et al., U.S. Patent No. 6,255,698 (“Gardner”). This rejection is respectfully traversed.

Gardner ‘698 relates to a method of forming “an integrated circuit in which gate structures for n-channel and p-channel transistors are separately optimized.” (Col. 1, lines

10-13). According to Gardner, “a p-type active region 12 and n-type active region 14 [are] formed within substrate 10.” (Col. 8, lines 1-2; Fig. 1). Gardner ‘698 teaches that “[a]ctive region 12 may be separated from active region 14 and other adjacent active regions by isolation regions 16.” (Col. 8, lines 3-4; Fig. 1). Gardner ‘698 also teaches that a “gate dielectric layer 18 is formed over the upper surface of substrate 10” and “[c]onductive . . . layer 22 is formed above dielectric 18.” (Col. 8, lines 4-7; Fig. 1). According to Gardner ‘698, “[g]ate structures are patterned from layers 18, 20 and 22” such that “[g]ate structure 24 is formed over p-type active region 12, and gate structure 26 is formed over n-type active region 14.” (Col. 8, lines 60-63; Fig. 2). Thus, Gardner ‘698 teaches the formation of trench 16 before the formation of gate structures 24, 26.

The subject matter of claims 10 and 11 would not have been obvious over Lu in view of Gardner. Specifically, the Office Action fails to establish a *prima facie* case of obviousness. Courts have generally recognized that a showing of a *prima facie* case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. See e.g., In re Dembiczak, 175 F.3d 994, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 1355, 47 U.S.P.Q.2d 1453, 1456 (Fed. Cir. 1998); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573, 37 U.S.P.Q.2d 1626, 1630 (Fed. Cir. 1996).

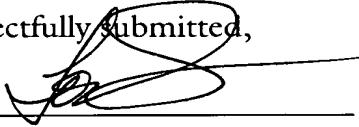
Neither Lu nor Gardner, whether considered alone or in combination, teach or suggest all limitations of claims 10 and 11. As noted above, Lu does not teach or suggest a “method for forming a coplanar waveguide” by “forming two longitudinal ground conductor planes over said substrate and on opposing sides of said signal conductor line,” as recited by amended independent claim 1, from which claims 10 and 11 depend. Likewise, Gardner, even when considered in combination with Lu, fails to teach or suggest a “method for forming a coplanar waveguide” by “forming two longitudinal ground

conductor planes over said substrate and on opposing sides of said signal conductor line," much less "subsequently forming a trench in said substrate in an area between at least one of said ground conductor planes and said signal conductor line," as recited in amended independent claim 1. For at least these reasons, the Office Action fails to establish a *prima facie* case of obviousness and withdrawal of this rejection is respectfully requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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